AD-A191 165 HYBRID PV HGCDTE IR DETECTORS TECHNOLOGY RELIABILITY & FAILURE PHYSICS PR..(U) HONEYWELL ELECTRO-OPTICS DIV LEXINGTON MA 27 MAR 87 N00014-86-C-2554 1/1

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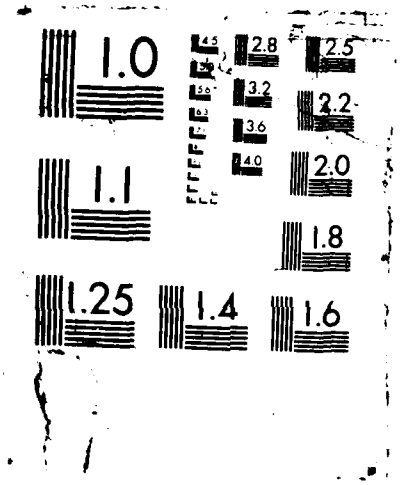
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HYBRID PV HgCdTe IR DETECTORS TECHNOLOGY RELIABILITY & FAILURE PHYSICS PROGRAM

ENVIRONMENTAL STRESS TESTING PLAN

TO
NAVAL RESEARCH LABORATORY

CONTRACT NO
N00014-86-C-2554

27 MARCH 1987

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Hybrid PV HgCdTe IR Detectors:
Technology Reliability and Failure Physics Program
Enviromental Stress Testing Plan

The objective of this test plan is to identify failure mechanisms in hybridized (indium bump interconnected) HgCdTe/Si focal plane arrays created by hybridization and environmental stress. Hybridization and environmental stresses identified in the statement of work to be addressed are;

1. Repetitive temperature cycling between 300K and 80K
2. Dewar bakeout
3. Dormant storage for several weeks at 130F
4. Long term storage (Honeywell believes the contract is not long enough to address long term storage)
5. Hybridization force (dislocation density versus R_oA)

In the plan both test arrays and focal planes will be stressed and characterized. Focal planes will be used to evaluate imaging performance while test arrays (interconnected to Si leadout boards) will be used to analyze changes in device performance by allowing the current voltage characteristics of individual photodiodes to be analyzed. In the text of this plan the word characterize is used. Table 1 describes the measurements and analysis performed on test arrays and focal planes when the word characterize is used. A summary of the device type and number of devices to be used in each stress test is shown in Table 2.

After a test array has recieved a series of stresses, elements will be analyzed to identify the mechanism of failure. For example, if a test array has a large loss of interconnect it might be destructively pulled apart and analyzed using an SEM to determine where the loss of interconnect is occurring.

1. Repetitive temperature cycling from 300K to 80K

Repetitive temperature cycling will be performed on focal plane arrays and test arrays.

Test arrays bump interconnected to silicon leadout boards will be used to evaluate the affect of temperature cycling on photodiode performance. Their evaluation will include interconnect yield, RoA, diode IV curves, noise, and responsivity. In addition to the interconnect yield a percent failure of detectors will be given where failures are based on the following criteria;

(1) a series resistance increase of a factor of 2 or

(2) a decrease of 25% or more in quantum efficiency or

(3) a reduction in R_0A by a factor ≥ 5.

Larger focal planes will also be temperature cycled. Their evaluation will include interconnect yield, responsivity, noise, and detectivity at 80k. Figure 1 is a diagram showing the intended test procedure. Honeywell intends to perform this procedure on; two test arrays, two 240 x 8 arrays hybridized to silicon leadout boards (50 elements tested) and one 240 x 8 focal plane array.

2. Dewar Bakeout

A typical dewar bakeout for insuring vacuum life of common module (HgCdTe photoconductor) dewars is 71 C for two weeks. It is generally the detector which limits the temperature at which dewars can be baked out. Honeywell intends to bakeout test arrays and focal planes at 71 C,
85 C and 100 C for periods of up to two weeks. Arrays will be characterized after the first 24 hours and then at the end of the bakeout schedule. See Figure 2. Honeywell intends to perform this test on two test arrays and two 240 x 8 arrays hybridized to silicon leadout boards.

In addition, several test structures will be baked to directly measure contact resistance and material interdiffusion.

3. Dormant Storage of Several Weeks at 130 F (54.4 C)

Stresses induced by storage at elevated temperatures will be evaluated by

vacuum baking test arrays and focal planes which have recieved a dewar bakeout and will thus already be characterized. Devices will be baked at 54.4 C for a minimum of two weeks to a maximum of four weeks and then will be recharacterized to assess any changes in array performance. Potentially two test arrays and two 240 x 8 arrays interconnected to silicon leadout boards will be evaluated.

4. Long term storage

Long term storage effects will not be evaluated on this program due to the programs length and emphasis on other environmental stresses. However, ZnS passivated, ion implanted photodiodes on MWIR LPE HgCdTe/CdTe (very similar to the devices used on this contract) were reported to be stable after storage for more than one year in air at room temperature in [1].

5. Hybridization force (dislocation density versus photodiode R_0A)

Honeywell is supplying ten 32 x 32 arrays which will be hybridized with a range of forces from 2×10^5 gm/cm^2 to 2×10^6 gm/cm^2. 32 elements of each array will be characterized and a map of R_0A will be established. The arrays will then be lapped to remove the CdTe substrate and a modified Polisar etchant will be used to establish an etch pit density map. The two maps will then be compared to determine if a correlation between dislocation density and photodiode R_0A exists.

References

[1] G. M. Williams
Stability of MWIR HgCdTe Photodiodes
Proc. IRIS Detector, May 1981

Measurements and Analysis Performed for Characterization

	Focal Plane Arrays	Test Arrays (24 elements)
Interconnect yield	CAMAT*	all elements
I-V Curves	2 photodiodes on each focal plane	all elements
Ro	from I-V curve	from I-V curves
RoA	from Ro and spot scan done on test array	from Ro and spot scan of a typical detector
Noise	CAMAT*	mostly from $(4KT/Ro)^{1/2}$
Blackbody Responsivity	CAMAT*	1000K, all elements
Spectral Response	CAMAT*	Nicolet FTS 5 elements/array
Detectivity (D*)	CAMAT*	Calculated from above

*Honeywells Computer Aided Mosaic Array Test Station

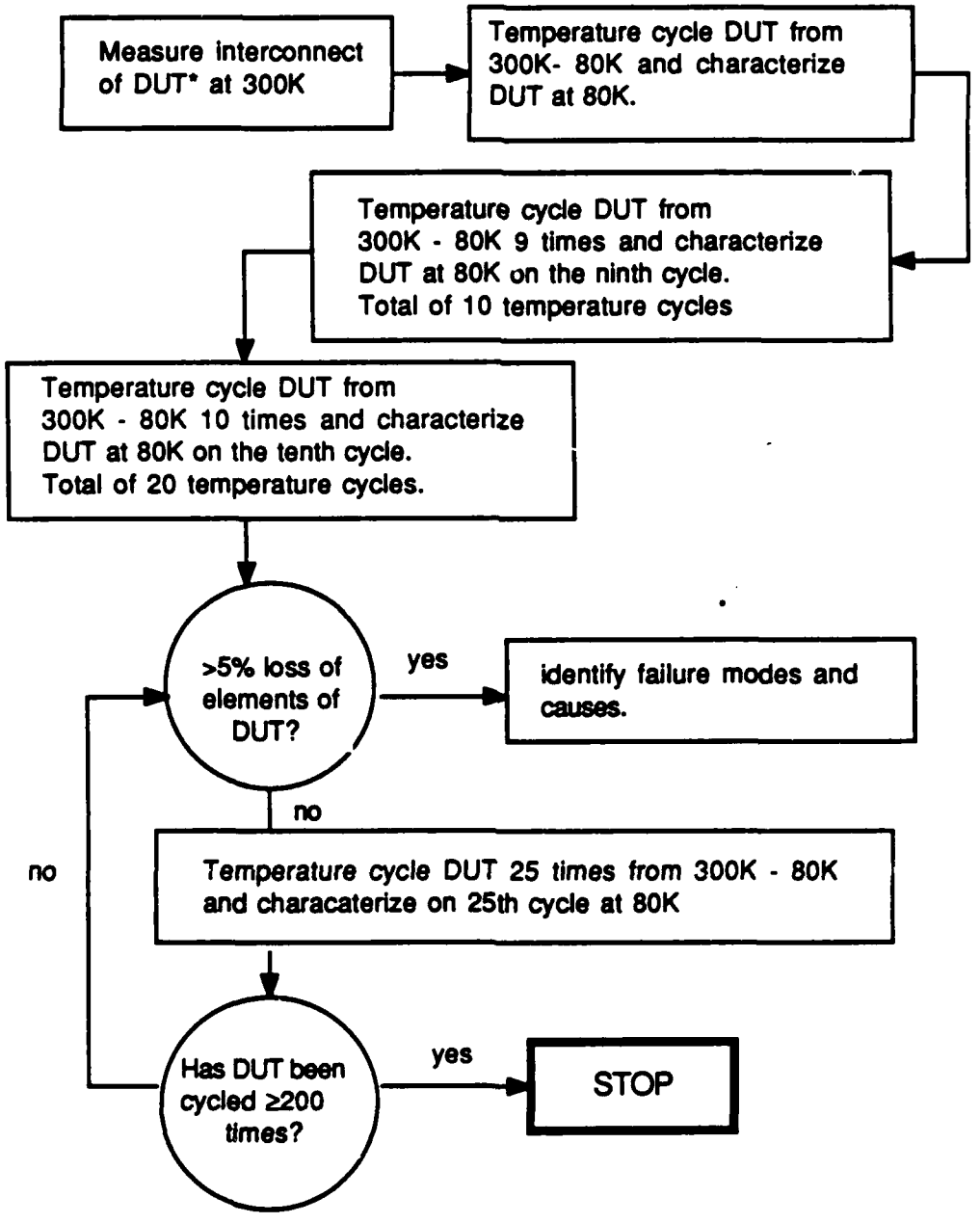
Table 1.

TABLE 2

of Arrays to be Subjected to Each Stress Test

Type of Device	Temp Cycled	Dewar Bakeout	Dormant Storage	R_o vs EPD
Test Array ~ 24 elements	2	2	2	
240 x 8 on silicon leadout board ~50 elements	2	2	2	
240 x 8 on Si MUX	1	1	1	
32 x 32 Array on leadout board				10

Temperature Cycling Test Plan For Focal Plane Arrays and Test Arrays



*device under test

Figure 1.

Vacuum "Dewar" Bakeout Test Plan for Focal Plane Arrays and Test Arrays

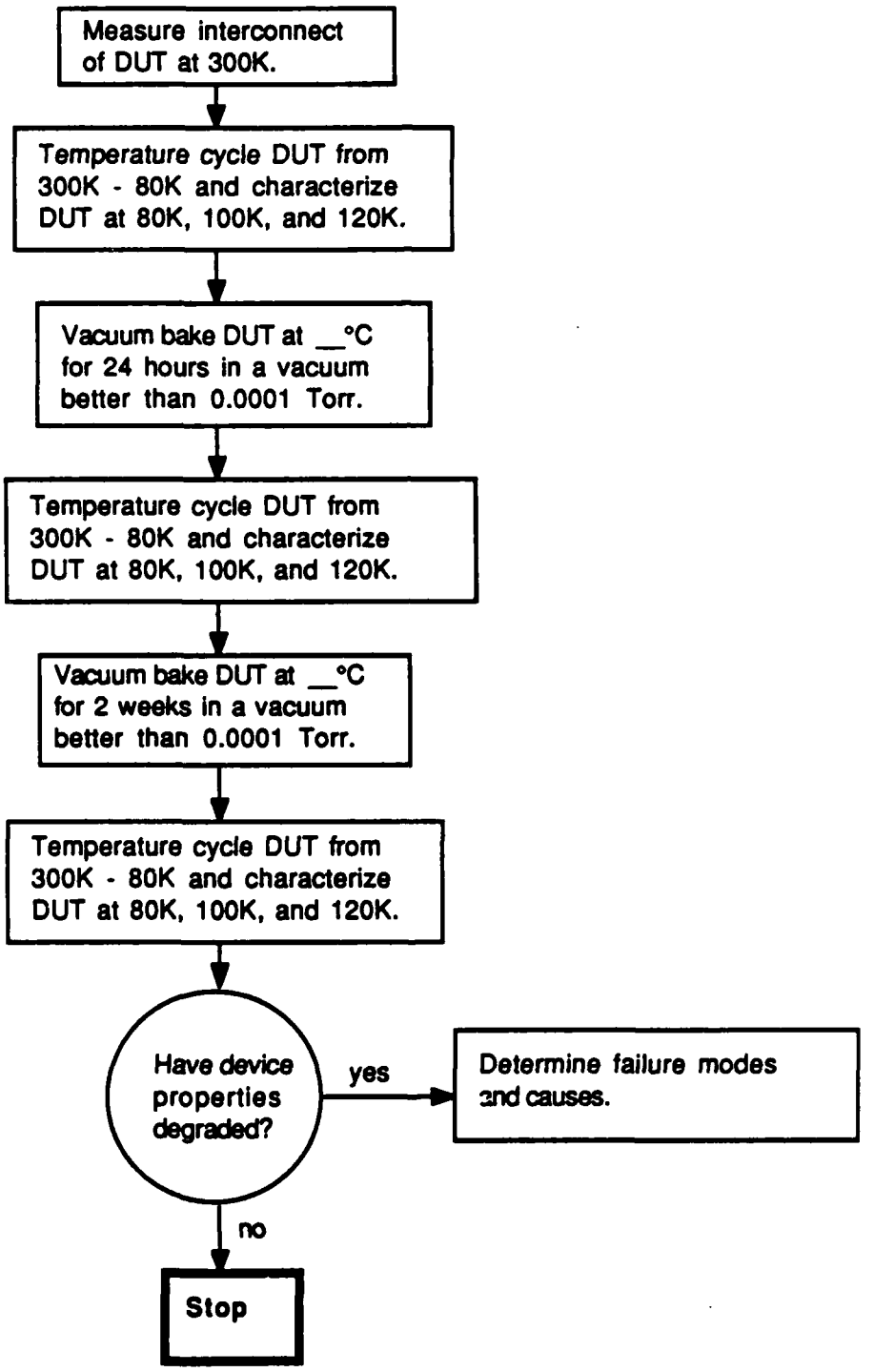


Figure 2.

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